REMARKS

Claims 1-18 are pending in the present application, claim 18 having been added herein. The Office Action and cited references have been considered. Favorable reconsideration is respectfully requested.

The disclosure and the claims were objected due to a number of informalities. These have been corrected. However, with respect to the Examiner's suggestion that Applicant provide a glossary, the Examiner's attention is invited to page 7 of the present specification, which provides a glossary of the terms referenced by the Examiner. Additionally, the abbreviations are preceded in the claims by the full element names to which they refer. Withdrawal of the objections is respectfully requested.

Claims 9 and 14-17 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for allegedly failing to particularly point out and distinctly claim the subject matter which the subject matter which Applicant regards as the invention. The claims have been amended to overcome this rejection. In claim 9, the word "item" has been replaced by the word "position". This is the exact translation of the word from the German text. In claim 14, the words "the latter" have been replaced by "this logical block address", as it makes the meaning clearer. Additionally, claim 14 now includes a recitation that the index table is associated with the mark "sector table" and that the search table is associated with the mark "sector mask". This is derived from the description page 3, lines 18 to 22. Withdrawal of this rejection is respectfully requested.

Claims 1-9 and 12-13 are rejected under 35 U.S.C. §102(b) as being anticipated by Estakhri et al. (U.S. Patent No. 5,930,815). Claims 10-11 were rejected

under 35 U.S.C. §103(a) as being unpatentable over Estakhri in view of Asnaashari (U.S. Patent No. 5,928,370). Claims 14-15 and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Estakhri in view of Kobatake (U.S. Patent No. 5,815,441). Claim 16 was rejected under 35 U.S.C. §103(a) as being unpatentable over Estakhri and Kobatake and further in view of Chen (U.S. Patent No. 6,456,528). These rejections are respectfully traversed for the following reasons.

Claim 1 recites a method for writing memory sectors in individually-deletable memory blocks (SB), comprising a number of memory sectors, whereby access to the physical sectors is achieved by means of an allocation table (ZT) for address conversion of a logical address (LA) into a physical block address (RBA) and a physical sector address (RSA), and whereby when a sector write command is to be carried out, which relates to an already written sector, the writing takes place to an alternative memory block (AB) by means of an altered address conversion, wherein the writing processes for sectors in the alternative memory block are carried out sequentially and the position of the relevant sector in the alternative block (AB) is stored in a sector table. This is not taught, disclosed or made obvious by the prior art of record.

Applicant respectfully submits that Estakrhi does not teach the method of the present application. The present application is related to flash memory devices, which are organized in blocks and these blocks are organized into sectors, where the sectors are writable individually into erased memory cells. The blocks are individually erasable, but not the sectors. If a sector has to be written a second time, this has to be done in another block.

A common technique is to write the new information of the addressed sector to an alternate block and if the sector in this block is also not erased, to join the original block and the alternate block in a third erase block. The other two blocks can then be erased. One feature of the present application is the writing of new information to written sectors of a block to sectors of an alternate block in a sequential manner, regardless of the sector address. The next free sector in the alternate block is used. This method is adapted to newer flash memory devices, where the writing of sequential sectors is performed at a higher writing speed.

Estakrhi does not handle the individual writing of sectors. The patent only speaks of erasable blocks (column 2, line 65-67) that can be written. Individually writable sectors are not mentioned. It is only stated that the blocks together with their sectors are written (column 14, lines 45 *et seq.*). In this case, the sectors are written of course sequentially, but this can only be done in completely erased blocks.

The blocks are handled by a space manager (544), which searches for a free block. The free block can be the next physical block, but also another one. *See, e.g.*, col. 71, line 65-col. 72, line 8. The examples in the description use, by chance, the next physical block if it is erased. There is no suggestion that writing to the next physical block has an advantage. One large table handles all the management of the blocks.

In contrast, the present application uses different tables for the address translation between logical and physical blocks and for the management of writing sectors. The second tables are very short and can be handled easily with a high speed. In claim 1, this is reflected in the recitations that "access to the physical sectors is achieved by means of an allocation table (ZT) for address conversion of a logical address

(LA) into a physical block address (RBA) and a physical sector address (RSA)," and "the position of the relevant sector in the alternative block (AB) is stored in a sector table." These features, in the claimed combination as set forth in claim 1, are not taught or suggested in Estakhri. For at least these reasons, Applicant respectfully submits that claim 1 is patentable over the prior art of record.

With respect to claims 10 and 11, Asnaashri is related to the secure erase of blocks in a flash memory where a block can contain sectors of 256 bytes. This is very common and neither special to the patent of Asnaashri nor to the present application. Claims 10 and 11 relate to block sizes and table sizes for the management of writing sectors to the flash memory. Asnaarshi, whether alone or in combination with Estakhri, does not speak about such tables.

With respect to claims 14-15 and 17, Kobatake relates to the combination of a flash memory with an EEPROM. It teaches that the EEPROM is byte by byte writable. That is not in the scope of the present application. Kobatake, whether taken alone or in combination with Estakhri, does not deal with the tables for the management of writing sectors to a flash memory, such as the search table, index table and sector table recited in claims 14-15 and 17.

Claims 2 -17 depend from an included recitation of claim 1. Applicant respectfully submits these claims are patentable of and of themselves, and at least for the reasons discussed above with respect to claim 1.

In view of the above amendments and remarks, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections of record.

Applicant submits that the application is now in condition for allowance and early notice to this effect is most earnestly solicited.

If the Examiner has any questions, he is invited to contact the undersigned at 202-628-5197.

Respectfully submitted,

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